**LIST OF FIGURES**

**FIG NO: FIGURE NAME PAGE NO**

1. Fig (2.1) : 4T SRAM Cell 4
2. Fig (2.2) : 4T SRAM Cell in idle mode when “0” is stored 4
3. Fig (2.3) : Buffered bit-lines 10
4. Fig (2.4) : Memory data-bus 10
5. Fig (3.1) : 6T SRAM Cell 14
6. Fig (3.2) : 4T SRAM Cell 16
7. Fig (3.3) : Voltage levels at the beginning of the read “0” operation 18
8. Fig (3.4) : Voltage levels at the beginning of the write “0” operation 20
9. Fig (3.5) : Sub-threshold leakage in NMOS transistor 22
10. Fig (3.6) : Variation of minority carrier concentration 22
11. Fig (3.7) : Change in VTH with N-well biasing 25
12. Fig (3.8) : 4T layout with two N-wells 26
13. Fig (4.1) : Layout of Row decoder circuit 30
14. Fig (4.2) : Layout of write circuit 31
15. Fig (4.3) : Schematic of 6T Sense amplifier 32
16. Fig (4.4) : Layout of structural unit of 4T write circuitry 33
17. Fig (4.5) : Schematic of 4T Sense amplifier 34
18. Fig (5.1) : Divided Bit-line approach 36
19. Fig (5.2) : RC model 38
20. Fig (5.3) : Variation of delay with change in grouping 39
21. Fig (6.1) : Layout of 6T SRAM cell 41
22. Fig (6.2) : Simulation waveforms for 6T SRAM cell 41
23. Fig (6.3) : Layout of 4T SRAM cell 42
24. Fig (6.4) : Simulation waveforms for 4T SRAM cell 42
25. Fig (6.5) : Layout of 6T cache 44
26. Fig (6.6) : Simulation waveforms for 4T cache 44
27. Fig (6.7) : Layout of 6T sense amplifier 45
28. Fig (6.8) : Simulation waveforms for 6T sense amplifier 45
29. Fig (6.9) : Layout of 4T SRAM cache 46
30. Fig (6.10): Simulation waveforms for 4T cache 46
31. Fig (6.11) : Layout of 4T sense amplifier 47
32. Fig (6.12) : Simulation waveforms for 4T sense amplifier 47
33. Fig (6.13) : Layout of 4T divided bitline M=12 49
34. Fig (6.14) : Layout of 4T SRAM single bit line 50
35. Fig (6.15) : Simulation waveforms for 4T divided bitline M=12 51
36. Fig (6.16) : Simulation waveforms for 4T single bitline 51